

WHAT IS CLAIMED IS:

1 1. A method of buffering an RF signal comprising:
2 receiving an input signal, wherein the input signal alternates between a first
3 polarity and a second polarity;

4 generating a first current, wherein the first current is proportional to the input
5 signal when the input signal has the first polarity, and approximately equal to zero when the
6 input signal has the second polarity;

7 generating a second current, wherein the second current is proportional to the input
8 signal when the input signal has the second polarity, and approximately equal to zero
9 when the input signal has the first polarity;

10 generating a third current proportional to the first current;

11 generating a fourth current proportional to the second current;

12 applying the first and fourth currents to a first terminal of an inductor; and

13 applying the second and third currents to a second terminal of the inductor.

1 2. The method of claim 1 wherein a capacitance is between the first
2 terminal of the inductor and the second terminal of the inductor, and the inductor and
3 capacitance form a tank circuit.

1 3. The method of claim 2 wherein the input signal alternates between the
2 first polarity and the second polarity at a first frequency, the tank circuit has a resonant
3 frequency of a second frequency, and the first frequency and second frequency are
4 approximately equal.

1 4. The method of claim 2 wherein the first current and the second current
2 are generated by NMOS devices.

1 5. The method of claim 4 wherein the third current and the fourth current
2 are generated by PMOS devices.

1 6. The method of claim 2 wherein the first current is geometrically
2 proportional to the input signal when the input signal has the first polarity, and the second
3 current is geometrically proportional to the input signal when the input signal has the second
4 polarity.

1 7. A circuit for buffering RF signals comprising:
2 a first switch coupled between a first supply node and a first output node;
3 a second switch coupled between the first supply node and a second output
4 node;
5 a third switch coupled between the first output node and a second supply node;
6 a fourth switch coupled between the second node and the second supply node;
7 and
8 an inductor coupled between the first output node and the second output node.

1 8. The circuit of claim 7 wherein the first switch, the second switch, the
2 third switch, and the fourth switch are open or closed depending on the polarity of an input
3 signal.

1 9. The circuit of claim 8 wherein when the input signal has a first
2 polarity, the first and fourth switches are open, and second and third switches are closed.

1 10. The circuit of claim 9 wherein when the input signal has a second
2 polarity, the first and fourth switches are closed, and second and third switches are open.

1 11. The circuit of claim 7 wherein the third switch and the fourth switch
2 are NMOS devices.

1 12. The circuit of claim 11 wherein third and fourth switch are biased near
2 their cutoff region.

1 13. The circuit of claim 11 wherein the first switch and the second switch
2 are PMOS devices.

1 14. The circuit of claim 13 wherein the PMOS devices are configured to
2 provide positive feedback.

1 15. An integrated circuit, wherein the integrated circuit comprises the
2 circuit of claim 7.

1 16. A circuit for buffering RF signals comprising:
2 a first device coupled between a first output node and a first supply node,
3 having a control electrode coupled to a first input node;

4 a second device coupled between a second output node and the first supply
5 node, having a control electrode coupled to a second input node;
6 a third device coupled between a second supply node and the first output node,
7 having a control electrode coupled to the second output node;
8 a fourth device coupled between the second supply node and the second output
9 node, having a control electrode coupled to the first output node; and
10 an inductor coupled between the first output node and the second output node.

1 17. The circuit of claim 16 further comprising:
2 a fifth device coupled between the first device and the first output node; and
3 a sixth device coupled between the second device and the second output node.

1 18. The circuit of claim 16 wherein the first device and the second device
2 are NMOS devices, and the third device and fourth device are PMOS devices.

1 19. An integrated circuit, wherein the integrated circuit comprises the
2 circuit of claim 18.

1 20. A transceiver comprising the circuit of claim 18.

1 21. An computing device comprising:
2 a memory;
3 a central processing unit coupled to the memory; and
4 the transceiver of claim 20 coupled to the central processing unit.